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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/657,482	09/08/2000	Eliyahou Harari	HARI.A06US3	9045

7590 05/24/2002

Skjerven, Morrill, Mac Pherson
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Suite 700
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EXAMINER
HUA, LY

ART UNIT	PAPER NUMBER
2131	10

DATE MAILED: 05/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

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27869 7590 03/18/2002

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Office Action Summary	Application No.	Applicant(s)	
	09/657,482	HARARI ET AL.	
	Examiner	Art Unit	
	Ly V. Hua	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *64-119* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *64-89* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *90-119* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *7 and 8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restriction

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:
   - I. Claims 63-89, drawn to a memory system in which a write cache memory is used, classified in class 711, subclass 118.
   - II. Claims 90-119, drawn to a method of operating a memory system which does not include a write cache memory, classified in class 714, subclass 8.

2. The inventions are distinct, each from the other because of the following reasons: Inventions of Group I and Group II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention of Group II has separate utility such as it in an enviornment where caching is not necessary. See MPEP § 806.05(d).

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

5. During a telephone conversation with Mr. Gerald P. Parsons (Reg. No.: 24,486) on January 9, 2001, a provisional election was made without traverse to prosecute the invention of Group I, claims 63-89. Affirmation of this election must be made by applicant in replying to this Office action. Claims 90-119 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

6. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

7. Claims 80-89 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

   a. With regard to claim 80 (and thus its dependent claims 81-89):
      - i. The phrase "said at least one array" lacks antecedent basis.
      - ii. The phrase "said removed data" (in the last line) lacks antecedent basis.
      - iii. The phrase "the memory array" (in the last line) lacks antecedent basis.

   Since antecedent basis problems exist as shown above, the applicant is requested to review and correct all other antecedent basis problems in other claims if detected.

8. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 U.S.C. § 102(f) or (g) prior art under 35 U.S.C. § 103.

10. Claims 63, 71,, 73, 80 and 83 are rejected under 35 U.S.C. § 103 as being unpatentable over Fukushi et al. (4,757,474, hereafter referred to as Fukushi) in view of Rao (4,949,309) and common practices in the art.

a. As per claims 63, 71, 73, 80 and 83:
   i. Fukushi teaches a storage memory system [Fig. 3] that is inherently connectable to a host system, comprising:
      (1) an array [1]
         (a) of memory cells
         (b) arranged to store
            (i) in designated blocks (groups or sectors) thereof; and
      (2) a controller [combination of elements 2-6]
         (a) inherently connectable to a host system,
         (b) for controlling operation of
            (i) the array and
         (c) including:
            (i) an addressing circuit [combination of elements 2-6]
               1) responsive to receipt
                  I of a mass memory storage block address [Am1 ... Ao]
                  II from the host system
               2) to generate [by element 3]
                  I an address of at least one corresponding array block (group or sector),
               3) being responsive
                  I to a list [5] of array blocks that have other array blocks substituted therefore
                  II to substitute at least one address of such other array blocks for the generated address of said at least one array {block}.
   ii. However, Fukushi,
      (1) whose attention is toward memory block substitution, without concerning about a well known feature of caching data between a host system and his storage memory system,
      (2) does not explicitly teach:
         (a) that his storage memory system [Fig. 3] comprises
            (i) a cache memory separated from the array;
         (b) that his controller includes
            (i) *an erasing circuit*
               1) that causes
                  I all of the memory cells of one or more designated blocks of the array to be erased together,
            (ii) a first data transfer circuit
               1) responsive to the addressing circuit

2) to execute an instruction from the host system
3) to perform a designated one of
I (1) a data write operation by writing user data to the cache memory, or
II (2)a data read operation by reading
{1} addressed user data
{a} first from the cache memory, if stored therein, or
{b} from the array, if not stored in the cache memory, and

(iii) a second data transfer circuit
1) that removes
I data
II from the cache
III by writing said removed data in to the memory array.

iii. Rao teaches:
(1) *an erasing circuit*
(a) that causes
(i) all of the memory cells of one or more designated blocks of the array to be erased together.
(2) in that Rao teaches a plurality of flash EEPROM memory cells
(a) which are partitioned into
(i) groups (or sectors),
1) each of which groups comprises
I a plurality of storage cells that can be individually addressed for individually programming and erasing each of the storage cells without disturbing the other storage cells.

iv. Bastian teaches [in his Fig. 1, and col. 3 line 60 to col. 4, line 19]:
(1) a first data transfer circuit
(a) responsive to the addressing circuit
(b) to execute an instruction from the host system
(c) to perform a designated one of
(i) a data write operation by writing user data to the cache memory, or
(ii) a data read operation by reading
{1} addressed user data
{a} first from the cache memory, if stored therein, or
{b} from the array, if not stored in the cache memory, and

(2) a second data transfer circuit
(a) that removes
(i) data
(ii) from the cache
(iii) by writing said removed data in to the memory array.

v. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to:

(1) implement
  (a) a memory device having Rao's EEPROM cells
  (b) using
    (i) Fukushi's teaching of substituting spare storage cells for regular storage cells and
    (ii) Rao's teaching of using:
      1) flash EEPROM cells as a storage cells and
      2) erasing circuit for erasing flash EEPROM.

vi. The person having ordinary skill in the art would have been motivated to combine the teachings of Rao, Fukushi and Bastian **because** :
  (1) with regard to memory patching/substituting/masking,
    (a) the person would wish to substitute a spare storage cell for a regular storage cell when the regular storage cell cannot be acted on as taught by Fukushi, and
    (b) that person would know that EEPROM cells are like any other kind of memory cells are some time cannot be acted on due to defect; and
  (2) with regard to memory cache/buffer such as that of Bastian,
    (a) using caching/buffering to store more frequently used data is a common practice in the art,
    (b) using caching/buffering to open up bottle neck of writing to slow memory is well known in the art; and
    (c) Bastian does teach data transfer circuits necessary for transferring data among host system, cache memory and memory that is relatively slower then the cache memory; and
  (3) the combination would
    (a) provide:
      (i) memory reliability,
      (ii) memory fast operation
      both of which are commonly expected from a computer memory device; and
    (b) enhance processing time efficiency at the source which sends the data.

b. <u>As per claims 64, 72, 76, 77, 78, 81, and 82:</u>
  i. The features recited in these claims are known as of a "first-in-first-out" buffer/cache (which cache is often a volatile memory since it is fast to operated).
  ii. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use such known cache for the same fast flushing purpose.

c. <u>As per claims 65, 66, 67, 68, 79 and 87:</u>
  i. Official Notice is hereby taken that storing overhead data (such as error correction code, error detection code, attributes and/or directive information) with its associated data is common practice in the art.
  ii. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to store overhead data with data in a memory device so that the overhead data can be used to correct/detect error in the data as well known in the art.

d. <u>As per claim 85</u> :
  i. An amount of user data of 512 bytes is typical size.
  ii. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to select 512 bytes as an amount of user data and implement as memory area accordingly to store such amount of data.

e. As per claims 74 and 86:

i. The features recited in the parent claims 71 and 80 of these claims have been addressed above with the reason of obviousness.

ii. These claims 74 and 86 recite that the mass/bulk storage memory system is implement in a single card/package that is removably connectable to the host system through an electrical connector.

iii. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to integrate the combination of Fukushi, Rao and Bastian in a single card because the advancement in semiconductor technology enable many associated elements to be implement is a single chip/card.

iv. The artisan would have been motivated to integrate the combination of Fukushi, Rao and Bastian in a single card because such single card is more modular and compact.

f. As per claims 69, 70, 88 and 89:

i. The features recited in the parent claims 63 and 80 of these claims have been addressed above with the reason of obviousness.

ii. These claims recite that in the mass/bulk storage memory system the first and second data transfer circuits write data into the memory cell array with exactly two programmable states per memory cell storage element, thereby to store exactly one bit of data per storage element.

iii. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize that a memory is programmable with exactly two states, state 1 (2.5V<Voltage<2.5V for one high/true logic state) or a state 0 (0V<Voltage<2.5V for one low/one logic state).

11. Claim 75 is rejected under 35 U.S.C. § 103 as being unpatentable over Fukushi, Rao and Bastian as applied to claim 83 above and further in view of Tuma et al (5,070,474 hereinafter referred to as Tuma).

a. As per claim 75:

i. A controller (i.e., the SMD disk controller, which see a solid state memory as a disk), which is **interfaced** with a solid state memory, for responding to commands sending to a disk and for controlling the solid state memory (col. 4, lines 9-37).

ii. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to add Tuma's controller to the modified memory device of Fukushi.

iii. The artisan would have been motivated to add Tuma's controller to the modified memory device of Fukushi because:

(1) Fukushi's memory device is of solid state type;

(2) Tuma's memory is of solid state type; and

(3) The addressing of the solid state memory of Fukushi is similar to the addressing of the solid state memory of Tuma as it is expected in the art of addressing solid state memories.

12. Claim 84 is rejected under 35 U.S.C. § 103 as being unpatentable over Fukushi, Rao and Bastian as applied to claims 56 and 58 above and further in view of Takemae (4,688,219).

a. As per claim 84:

i. Takemae teaches:

(1) a means for correcting those error which can be corrected by using error correction codes.

ii. It would have been obvious to one having ordinary skill in the art at the time the invention was made
   (1) to combine the teaching of Takemae with the teachings of Rao, Fukushi and Bastian
   (2) to include in a memory-area-substituting list entries which indicates memory area in which data error cannot be corrected so that only those "non-correctable" memory areas can be substituted with good memory areas.

Double Patenting

13. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

14. Claims 74, 86, 69, 70, 88 and 89 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over the claims of U.S. Patent No. ~~5,764,888~~ 5,297,148.

15. As per claims 74 and 86:
   a. The features recited in the parent claims 71 and 80 of these claims have been addressed above with the reason of obviousness.
   b. These claims recite that the mass/bulk storage memory system is implement in a single card/package that is removably connectable to the host system through an electrical connector.
   c. Claim 44 of patent number 5,297,148 recites the same.
   d. Thus, if claims 74 and 86 of the present application are allowed, these claims would extend patent coverage of the claims of the patent 5,297,148.

16. As per claims 69, 70, 88 and 89:
   a. The features recited in the parent claims 63 and 80 of these claims have been addressed above with the reason of obviousness.
   b. These claims recite that in the mass/bulk storage memory system the first and second data transfer circuits write data into the memory cell array with exactly two programmable states per memory cell storage element, thereby to store exactly one bit of data per storage element.
   c. Claim 45 of patent number 5,297,148 recites the same.
   d. Thus, if claims 69, 70, 88 and 89 of the present application are allowed, these claims would extend patent coverage of the claims of the patent 5,297,148.

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

18. **Any response to this final action should be mailed to:**

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 746-7238, (for formal communications; please mark "EXPEDITED PROCEDURE")

Or:

(703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

19. The Examiner, hereby, requests that the Applicant would please provide (in addition to a normal response in hard copy) the Examiner an electronic **copy** of Applicant's response to this Office Action by E-mail it to the Examiner's E-mail address Ly.Hua@USPTO.GOV.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Ly Hua whose telephone number is (703) 305-9684. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gail Hayes, can be reached on (703) 305-3711. The fax phone number for this Group is (703) 305-3718.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-9600.

LY V. HUA
PRIMARY PATENT EXAMINER
ART UNIT 2131

L. Hua
March 11, 2002